ESDA/JEDEC Joint Standard

ANSI/ESDA/JEDEC JS-002-2022

ANSI/ESDA/JEDEC JS-002-2022

Revision of ANSI/ESDA/JEDEC JS-002-2018

For Electrostatic Discharge Sensitivity Testing

Charged Device Model (CDM) Device Level

Electrostatic Discharge Association
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Rome, NY 13440

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An American National Standard
Approved June 8, 2021

ESDA/JEDEC Joint Standard
For Electrostatic Discharge
Sensitivity Testing

Charged Device Model (CDM)
Device Level

Approved June 8, 2021
EOS/ESD Association, Inc. & JEDEC Solid State Technology Association

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Published by:

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Printed in the United States of America, ISBN: 1-58537-333-8

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(This Foreword is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Foreword

This joint standard[1] was developed under the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a joint working group composed of both ESDA and JEDEC.

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM, a device itself becomes charged (for example, by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. Similarly, a non-charged device can experience CDM stress as a charged conductive object approaches and discharges to the device. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges from other similar scenarios, such as the discharging of charged metal objects to devices at a different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the measuring equipment's limitations and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on many factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage. It has also been shown that the CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package may be less susceptible to CDM damage at a given voltage than that same IC in a package of the same type with a larger area. Clause 7.5 and Annex C address small package CDM and outlines the procedure to characterize small packages (by technology/common ESD design to those in larger packages, capacitance measurement) such that CDM testing for those small packages may not be needed.

New information includes a procedure to determine multiple level CDM withstand thresholds for subsets of device pins and a more accurate definition of verification module physical characteristics and capacitance measurement/use of modules.

[1] ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system, or process that also specifies the procedures for determining whether each of the requirements is satisfied.

Foreword (cont'd)

A companion technical report document, ESDA/JEDEC JTR002-01, has also been released to act as a "user guide" for this CDM test standard. The information presented in the user guide is intended to help users better understand the procedures and requirements specified in this standard.

References to the user guide are made throughout this standard to aid the reader in the practical elements of adhering to the requirements outlined in this document.

This standard is maintained and revised as a joint standard through a memorandum of understanding between JEDEC and ESDA. This standard is a living document, and revisions and updates will be made on a routine basis driven by the electronic industry's needs.

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Foreword (cont'd)

This document was originally approved on August 29, 2014 and was designated ANSI/ESDA/JEDEC JS-002-2014. ANSI/ESDA/JEDEC JS-002-2018 was a limited revision of ANSI/ESDA/JEDEC JS-002-2014 and was approved on February 16, 2018.

ESDA/JEDEC JS-002-2022 is a revision of ANSI/ESDA/JEDEC JS-002-2018 and was approved on June 8, 2021.

ESDA/JEDEC JS-002-2022 was prepared by the ESDA 5.3.1 Device Testing (CDM) subcommittee and the JEDEC JC14.1 ESD Task Group.

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Foreword (cont'd)

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CHARGED DEVICE MODEL (CDM)
DEVICE LEVEL

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CHARGED DEVICE MODEL (CDM)
DEVICE LEVEL

(From Board Ballot JCB-22-08 jointly formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee.)

1 Scope

This document establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin-film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. The devices shall be assembled into a package similar to that expected in the final application to perform the tests. This CDM document does not apply to socketed discharge model testers.

The purpose (objective) of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative References

Unless otherwise specified, the following documents of the latest issue, revision, or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices[3]

JESD88, Dictionary of Terms for Solid-State Technology[3]

JESD625, Requirements for Handling Electrostatic Discharge-Sensitive (ESDS) Devices[3]

ANSI/ESD S20.20, Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)[2]

IEC61340-5-1 – Electrostatics – Part 5-1: Protection of Electronic Devices from Electrostatic Phenomena – General Requirements[4]

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[2] EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937; www.esda.org

[3] JEDEC Global Standards for the Microelectronics Industry; www.jedec.org

[4] IEC – International Electrotechnical Commission, www.iec.ch

3 Terms and Definitions

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at www.esda.org.

above-passivation layer (APL). A low-impedance metal plane built on the surface of a die above the passivation layer connecting a group of bumps or pins (typically power or ground).

NOTE This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

charge time (delay). The amount of time the device is allowed to charge – any additional time is added to the default (set by the manufacturer) in most cases.

charged device model electrostatic discharge (CDM ESD). An ESD stress model that simulates the discharge event that occurs when a charged component is quickly discharged to another object at a different electrostatic potential through a pin.

charged device model (CDM) electrostatic discharge (ESD) tester. Equipment (referred to as "tester" in this standard) that simulates the device level CDM ESD event using the non-socketed test method.

C_{Small}: Device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below the determined value that CDM testing is not required if specified conditions are met.

dielectric layer. A thin insulator placed atop the field plate that is used to separate the device from the field plate.

discharge time (delay). The amount of time that the pogo pin remains in contact with the pin under test – any additional time is added to the default (set by the manufacturer) in most cases.

field plate. A conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling (see Figure 1).

ground plane. A conductive plate used to complete the circuitry for grounding/discharging the DUT (see Figure 1).

IPA. Isopropyl alcohol or isopropanol, with a minimum percentage of 70% alcohol.

no-connect pin. A package contact (pin, bump, or ball) that is not electrically connected to a die.

software voltage. A user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system to achieve the waveform parameters as defined in Table 1 or Table 2.

supply pin. Any device pin that provides operating current to that device.

NOTE Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current levels). For ESD testing, power and ground pins are treated as supply pins.

test condition (TC). For purposes of this document, a test condition refers to the tester plate voltage that meets the waveform parameter conditions in a particular column of Table 1 and Table 2.

4 Personnel Safety

THE EQUIPMENT SHALL NOT BE INSTALLED OR OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.

ALL PERSONNEL SHOULD RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING BEFORE USING THE EQUIPMENT.

THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.

GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.

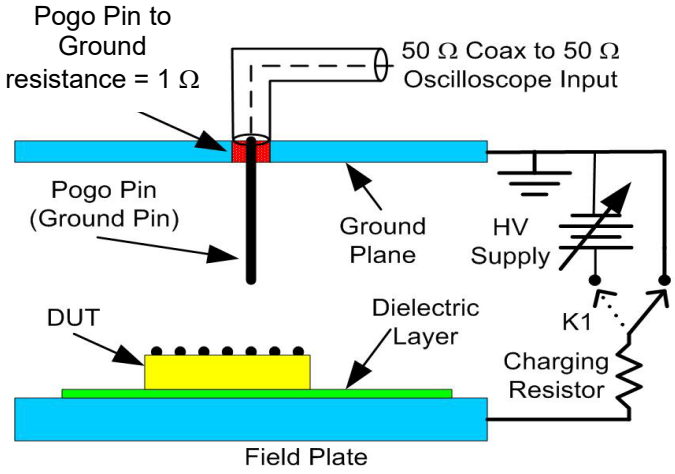
ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.

NOTE CDM testers have moving parts when in operation and care should be taken to avoid personnel contact with moving parts.

5 Required Equipment

5.1 CDM ESD Tester

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device, or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 ohm current path. When measuring waveforms, the 1 ohm pogo pin to ground connection of the resistive current sensor will be a parallel combination of a 1 ohm resistor between the pogo pin and the ground plane and the 50 ohm impedance of the oscilloscope and its coaxial cable. K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this standard shall meet the waveform characteristics specified in Figure 2, Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe assembly.



NOTE When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance, inductance, and capacitance (RLC) parasitics in the equipment greatly influence the test results.

Figure 1 — Simplified CDM Tester Hardware Schematic

5.1.1 Current Sensing Element

A current sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of 1.0 ohm ± 10%. A resistor, as specified in Clause 5.1, shall be used as the current sensing element. The value of resistance (including the 50 ohm cable and its termination) shall be measured using an ohm meter as described in Clause 5.5. The resistance value shall be used to calculate the peak currents.

The current sensing element shall have a minimum frequency response of 9 GHz (specified by maximum roll off of 3 dB at 9 GHz).

NOTE More information on the measurement of the current sensing element can be found in the user guide ESDA/JEDEC JTR002-01 “For the User Guide of ANSI/ESDA/JEDEC JS-002.

5.1.2 Ground Plane

The probe assembly shall contain a square ground plane with the probe pin centered within it, as shown in Figure 1. The dimensions of the ground plane shall be 63.5 mm x 63.5 mm $\pm$ 6.35 mm.

5.1.3 Field Plate/Field Plate Dielectric Layer

The field plate shall have a surface flatness to vary no more than 0.127 mm. The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0.381 mm $\pm$ 0.025 mm to result in a capacitance measurement (as specified in Annex B) in the range specified in Table 4 in Annex A.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table 4 in Annex A.

5.1.4 Charging Resistor

The charging resistor shown in Figure 1 shall nominally be 100 megohms or greater.

Resistor values higher than 100 megohms may be used, but this may not allow very large devices (refer to Clause 6.9 and Annex J) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 megohms, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for charging large devices. A procedure for this large device delay characterization is given in Annex J.

5.1 Waveform Measurement Equipment

The CDM waveform measurement equipment shall consist of the following components.

5.2.1 Cable Assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 5 GHz and a nominal 50 ohm impedance.

5.2.2 Equipment for High Bandwidth Waveform Measurement

5.2.2.1 High Bandwidth Oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and $\geq$20 gigasample/sec sampling rate with a nominal 50 ohm input impedance.

5.2.2.2 Attenuator

A 20 dB attenuator with a precision of ± 0.5 dB, at least 12 GHz BW, and an impedance of 50 ohms ± 5.0 ohms.

5.2.3 Equipment for 1 GHz Waveform Measurement

5.2.3.1 1 GHz Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 ohm input impedance. The sampling rate shall be ≥ 5 gigasample/sec.

NOTE The user can use a higher BW oscilloscope and use a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in Clause 5.2.3.1.

5.2.3.2 Attenuator

A 20 dB attenuator with a precision of ± 0.5 dB, at least 4 GHz BW, and an impedance of 50 ohms ± 5 ohms.

5.3 Verification Modules (Metal Discs)

The large verification module shall have a capacitance of 55 pF ± 13% and the small verification module shall have a capacitance of 7.2 pF ± 13%. Refer to Annex A for information on the verification module physical dimensions and Annex B for information on the capacitance measurement procedure.

5.4 Capacitance Meter

Capacitance meter with a resolution of 0.2 pF, measurement accuracy of 3%, and a measurement frequency of 1.0 MHz as described in Annex B.

5.5 Ohm Meter

The ohm meter used to measure the resistive probe's resistance shall be capable of measuring to an accuracy of 0.01 ohms using a Kelvin 4-wire connection.

6 Periodic Tester Qualification, Waveform Records, and Verification Requirements

6.1 Overview of Required CDM Tester Evaluations

The CDM tester shall be qualified, requalified, and periodically verified as described in this clause. The safety precautions described in Clause 4.0 shall be followed at all times.

NOTE Changes in the shape of the discharge pulse, even though they may still be within specification, may indicate degradation of the discharge path.

6.2 Waveform Capture Hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- Oscilloscope - as specified in Clause 5.2.
- Attenuator and cable assembly as defined in Clause 5.2.
- Verification modules (as described in Clause 5.3) - with the dimensions and attributes listed in Annex A and measurement methods listed in Annex B.

6.3 Waveform Capture Setup

The procedure for waveform capture setup follows these steps:

1) Clean the verification modules. Avoid skin contact with the modules before and during testing. A recommended procedure is described in Annex A.

2) Using an IPA wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.

3) Attach the appropriate 20 dB attenuator as described in Clause 5.2 to the oscilloscope. Attach one end of the external cable assembly, as described in Clause 5.2.1, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See Annex G for an example of oscilloscope settings and captured waveforms.

NOTE See also the ESDA/JEDEC JTR002-01 User Guide.

6.4 Waveform Capture Procedure

The procedure for waveform capture for a particular polarity follows these steps:

1) Place the verification module on the field plate dielectric and ensure intimate contact between the field plate dielectric and verification module. Whenever waveforms are captured, the verification module shall always be oriented with the same surface facing the dielectric; this surface must be the one resulting in the higher capacitance as described in Annex B.

2) Set the potential of the field plate to the needed voltage for the test condition being run.

3) Align the ground pin to approximately the center of the verification module.

4) Either the single discharge or dual discharge method described in Annex H.1 or Annex H.2, respectively, can be used, but the discharge method chosen should be consistent with how a product will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

5) Discharge the verification module at least ten times at the polarity being verified.

6) Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for first peak current (Ip), rise time (t_r), full width at half maximum (FWHM), and second peak current (Ip_2) for this group of waveforms as shown in Figure 2 (see Clause 6.7).

7) If the waveform characteristics do not meet the requirements defined in either Table 1 or Table 2 for the target test condition, re-clean the verification modules and ground pin, check that all connections are tight, adjust the field plate voltage, and repeat steps 6.4.1 through 6.4.7. See Clause 6.5 and Clause 6.6 for the appropriate table and test conditions to use.

NOTE If this still does not work, check the system vacuum, or replace the ground pin. Consult the tester manufacturer for more information.

8) Repeat the procedure for the opposite polarity.

6.5 CDM Tester Qualification/Requalification Procedure

The qualification/requalification procedure is performed to determine the field plate voltage needed for each test condition setting (125 – 1000) to produce peak currents in the ranges corresponding to Table 2, and therefore corresponding to the classification levels as specified in Table 3.

Two alternative procedures for qualifying and routinely checking the CDM test system are introduced in Annex I. These procedures are based on generally-available CDM test systems and offer two methods for adjusting the field plate voltage to meet the waveform parameters of Table 2.

CDM test system manufacturers or test system operators may develop alternate qualification procedures from the two procedures in Annex I, as long as these result in waveforms that meet the requirements of Table 2 for the various test conditions.

6.5 CDM Tester Qualification/Requalification Procedure (cont'd)

It is recommended that settings determined from this qualification procedure be recorded for a particular test system, oscilloscope BW and polarity. This allows for the detection of drift over time on the system, which may indicate a larger issue with the system. See Annex I.3 for examples.

Perform the setup and waveform capture steps described in Clause 6.3 and Clause 6.4 for Test Conditions 125-1000 in Table 2 for both positive and negative polarities using both small and large verification modules and measuring with the high bandwidth oscilloscope as specified in Clause 5.2.2.1. Refer to Annex I for flowcharts of the procedures.

NOTE If local site test voltage ranges will always be narrower than the range above (for example, Test Conditions 125-500), it is permissible to perform the qualification within that narrower range.

NOTE Further examples can be found in the ESDA/JEDEC JTR002-01 User Guide.

6.5.1 Conditions Requiring CDM Tester Qualification/Requalification

CDM tester qualification/requalification as described in this clause is required in the following situations:

- Acceptance testing when the CDM tester is delivered; usually performed by the manufacturer during installation.
- Periodic requalification per the manufacturer's recommendations. The maximum time between requalification tests is one year.
- After service or repair, that could affect the waveform.
- Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), and the discharge contacts (for example, pogo pins) are key elements of the tester construction. Any change to these elements requires a waveform verification.

6.5.2 1 GHz Oscilloscope Correlation with High Bandwidth Oscilloscope

During first acceptance testing, the tester manufacturer shall use a high bandwidth oscilloscope as specified in Clause 5.2.2.1 for initial waveform capture. If the test site only has a 1 GHz oscilloscope as specified in Clause 5.2.3.1, the tester manufacturer and end-user shall confirm that the user's oscilloscope measures tester waveforms as defined in Table 1 for quarterly and routine waveform acceptance. This is typically done using appropriate bandwidth filtering techniques and comparison with the oscilloscope from the tester manufacturer.

NOTE The Bessel-Thomson software filter option on many oscilloscopes is a recommended high bandwidth waveform filter as it aligns well with actual 1 GHz oscilloscope data.

Oscilloscope correlation verification shall be repeated if the test site changes 1 GHz oscilloscopes.

6.6 CDM Tester Waveform Verification Procedure

6.6.1 Quarterly Waveform Verification Procedure

Perform the setup and waveform capture steps as described in Clause 6.3 and Clause 6.4 under Test Conditions 125-1000 in Table 1 using the 1 GHz oscilloscope as specified in Clause 5.2.3.1 or Table 2 using the high bandwidth oscilloscope as specified in Clause 5.2.2.1. Both verification modules shall be checked at positive and negative polarities. The recommendation is to use the high bandwidth oscilloscope if the option exists. Refer to Annex I for flowcharts of the procedures.

NOTE If local site test voltage ranges will always be narrower than the range above (for example, Test Conditions 125-500), it is permissible to perform the qualification within that narrower range.

Tester waveform verification shall be performed at least once per quarter.

6.6.2 Routine Waveform Verification Procedure

Perform the setup and waveform capture steps described in Clause 6.3 and Clause 6.4 under Test Condition 500 in Table 1 (1 GHz oscilloscope) or Table 2 (high bandwidth oscilloscope) for both positive and negative polarities. Use the verification module that most closely corresponds to the size package that will be tested. Refer to Annex I for example flowcharts of the procedures.

After tester qualification or requalification, routine waveform verification should be completed at least once per shift. If CDM stress testing is performed on consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between routine waveform checks may be used if no changes in waveforms are observed for several consecutive checks. The test frequency and method chosen shall be documented. If at any time the waveforms no longer meet the specified limits, all ESD stress test data collected after the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

NOTE Users can refer to the ESDA/JEDEC JTR002-01 User Guide for quarterly and routine verification information.

6.7 Waveform Characteristics

The waveforms shall appear as shown in Figure 2 for both the positive and negative polarities. The average waveform parameters (including Ip) as gathered per Clause 6.4 shall meet the specifications in Table 1 for a 1 GHz oscilloscope and Table 2 for a high bandwidth oscilloscope. If a high bandwidth oscilloscope is used for qualification, quarterly, and routine waveform verifications, the 1 GHz requirements need not be considered.

Table 1 — CDM Waveform Characteristics for a 1 GHz Bandwidth Oscilloscope

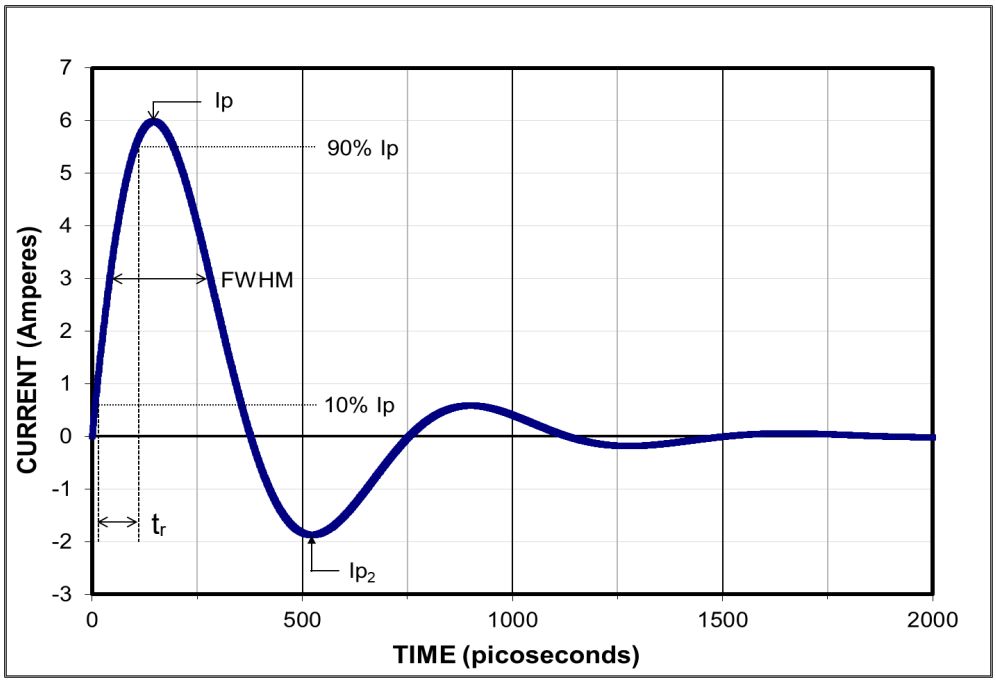
1 GHz BW Oscilloscope		Test Condition (hours)									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	Ip	1.0-1.6	1.9-3.2	2.1-3.1	4.2-6.3	4.4-5.9	9.1-12.3	6.6-8.9	13.7-18.5	8.8-11.9	18.3-24.7
Rise time (ps)	t_r	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450
Full width at half maximum (ps)	FWHM	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000	325-725	500-1000
Undershoot (A, max. 2nd peak)	Ip_2	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip

Table 2 — CDM Waveform Characteristics for a High Bandwidth (≥ 6 GHz) Oscilloscope

High BW (≥ 6 GHz) Oscilloscope		Test Condition (hours)									
		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	Ip	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	t_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	Ip_2	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip	< 70% Ip	< 50% Ip

NOTE The Test Condition 125-1000 voltages producing the specified peak current ranges are adjusted from JEDEC classification test voltages of 125, 250, 500, 750, and 1000 volts, respectively. Tester adjusted field plate voltages to achieve these current ranges for the ferrite free tester platform in this standard may vary somewhat between testers. Informative Annex E describes this relationship between JEDEC and ferrite free tester set voltages. Annex I describes two voltage adjustment methods.

6.7 Waveform Characteristics (cont'd)



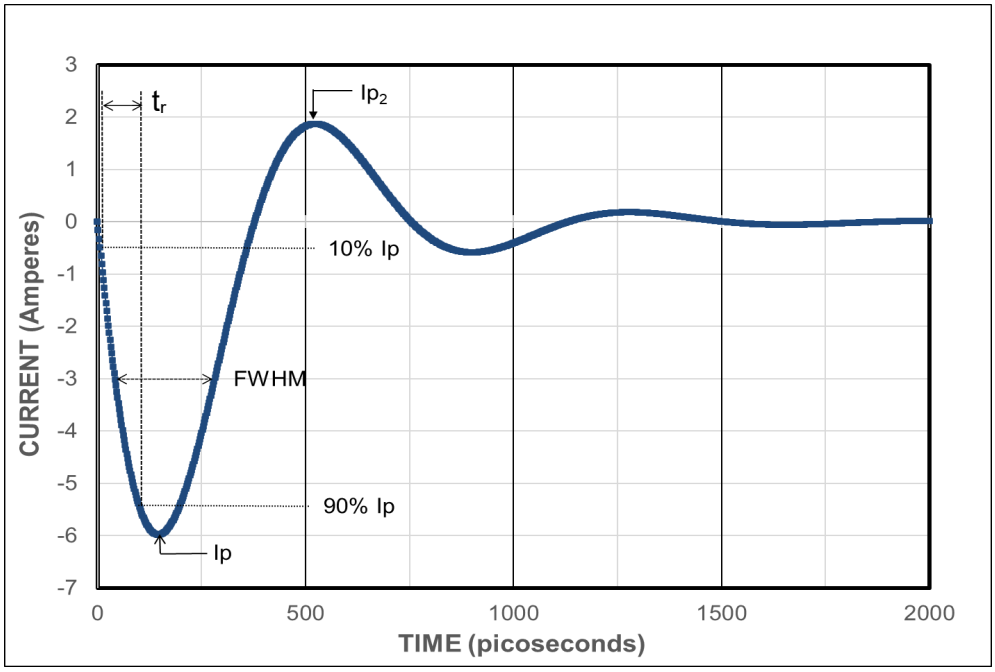


Figure 2 — CDM Characteristic Positive/Negative Waveforms and Parameters

6.8 Documentation

Retain the waveform records for tester qualification according to internal company policy. For tester requalification, quarterly waveform verification, and routine waveform verification, keep the records until the next set of waveforms are collected or according to internal company policy.

6.9 Procedure for Evaluating Full CDM Tester Charging of a Device

As defined in Clause 5.1.4, the charging resistor should nominally be 100 megohms or greater. If the resistor is too large, an added charging delay may be necessary to charge the device fully. To determine if an added delay is needed, follow the procedure in Clause 6.9 step 2).

Using the large verification module, follow these steps:

1) Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor Ip).
2) With the charge time set to 0 ms, collect ten waveforms and record the Ip from each. Calculate the average Ip of the waveforms.
3) With the charge time set to 500 ms, collect ten waveforms, record the Ip from each. Calculate the average Ip of the waveforms.
4) Compare the average Ip value from the 0 ms charge time and the 500 ms charge time measurements. If the average Ip for the 0 ms charge time is at least 95% of the average Ip for the 500 ms charge time, then packages with capacitance equal to or less than that of the large verification module will not require an added delay. If the average Ip for the 0 ms charge time is less than 95% of the average Ip for the 500 ms charge time, refer to Informative Annex J for a procedure to determine the appropriate charge time to ensure the device receives a full charge.
5) Even if the two average Ip values align, very large packaged devices (larger capacitance than the large verification module) may require a longer charge time delay to receive a full charge. Since device package technologies vary widely, there are no exact dimensions for how a particular package's Ip at a test condition may compare to the large verification module's Ip at the same test condition for the evaluation described above.
6) To determine if a very large packaged device may still require a longer charge time, step 1 through step 4 above can be repeated using the ground pin of a device. If the average Ip with 0 ms charge time and 500 ms charge time are not aligned, refer to Informative Annex J for a procedure to determine the appropriate charge time.

NOTE CDM testers have moving parts when in operation, and care should be taken to avoid personnel contact with moving parts when in operation.

7 CDM ESD Testing Requirements and Procedures

7.1 Tester and Device Preparation

Devices used for CDM stressing shall not have been used for any previous stress tests.

ESD damage prevention procedures shall be used before, during, and after CDM stressing and post parametric testing.

NOTE See the latest revision of ANSI/ESD S20.20, JESD625, IEC61340-5-1, or company-specific handling procedures for guidance.

7.1.1 Tester Cleaning

The CDM tester probe and field plate/dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using IPA.

NOTE Specific information on tester cleaning can be found in the ESDA/JEDEC JTR002-01 User Guide.

7.1.2 Device Cleaning

Devices should be cleaned with IPA before putting the device in the tester to improve waveform repeatability during CDM testing due to contamination of device terminals. Use a procedure approved by the local safety organization and following internal ESD handling procedures. A soft brush can be used to gently clean the device terminals paying attention to avoid bending pins or removing balls. Devices should then be handled in a way that maintains cleanliness (vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers which have been neutralized by holding in an ionized air stream). Cleaning with IPA may leave the surface moist for some time after the cleaning. The moisture may provide an unintended leakage path if present during the stress. It is important to dry all surfaces after cleaning, either by allowing sufficient time for the surfaces to dry or using forced airflow to evaporate the moisture.

Packages with an open cavity (for example, microphones) should be cleaned with particular attention to avoid IPA leaking into the package cavity. If this cannot be done, let the package dry longer after cleaning.

NOTE The cleaning process may be verified by stressing and measuring the peak current on several cleaned parts, comparing the same pins for peak current consistency.

7.2 Test Requirements

7.2.1 Test Temperature and Humidity

The test should be carried out at room temperature. Humidity at the test head should not exceed 30% RH. It is not intended to heat or cool the device during CDM testing.

NOTE Waveform repeatability is strongly dependent on the air's moisture content at the test head and having a low relative humidity will result in a more stable waveform.

7.2.2 Device Test

7.2.2.1 Pre-Stress Testing

Before ESD stressing, complete static and dynamic testing shall be performed on all submitted devices. Parametric and functional results shall be within limits specified in the datasheet parameters.

7.2.2.2 Failure Criteria

Following ESD stressing, complete static and dynamic testing shall be performed on all stressed devices. A device is considered to have failed if parametric and functional test results are not within limits specified in the datasheet parameters. A failure may be discounted if proven by failure analysis that it is not CDM–ESD related.

NOTE A change in static leakage (for example, pin leakage, standby current) is not an adequate criterion to determine pass/fail. It can serve as an indicator for the onset of damage.

NOTE If testing is to be done at multiple temperatures, perform the test first at room temperature, followed by cold temperature, then hot temperature (for example + 25°C, - 40°C, + 85°C).

7.3 Test Procedures

7.3.1 Sample Size

Unless otherwise specified, obtain a minimum of three samples that have been verified to meet the data specifications.

7.3.2 Initial Test Voltage

CDM testing should begin at the lowest level in Table 3 but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 3, and the device fails at the initial voltage, testing shall be restarted with three new devices at the next lower level.

7.3.3 Stressing the Pins

For each device, apply at least one positive and one negative discharge to each pin. Allow enough time (as specified in Clause 6.9) between discharges for the device to reach the full test voltage level. Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set shall have a minimum of three units.

7.3.4 Field-Induced Charging Method

There are two possible procedures for charging and discharging the device for the field-induced charging method: single and dual. Both procedures produce equivalent results. These procedures are described in Annex H. When testing products with no-connect pins using the dual discharge method, care must be taken to ensure that no-connect pins are stressed with both polarities because the DUT will not be charged to the opposite polarity by the first discharge.

NOTE See the ESDA/JEDEC JTR002-01 User Guide for more info on testing no-connect pins.

7.3.5 Allowance for Reduced Testing on Large Supply Pin Groups

If a supply pin group has a maximum pin-pin resistance of 1 ohm or less (see Clause 7.3.5.1), and the supply group pin count is greater than 10, as few as ten pins from that supply pin group can be used to represent the entire supply pin group for CDM testing. The remaining pins in the supply pin group need not be stressed. The ten pins for CDM testing shall be selected at random.

7.3.5.1 Supply Pin Groups

For this allowance, each supply pin is defined as a member of one and only one supply pin group. Supply pins interconnected by metal on the chip or within the package with a resistance of less than or equal to 1 ohm form a supply pin group. This connection includes pins connected on the package plane and/or by an above passivation layer (APL). If the pin interconnect design is unknown, the 1 ohm resistance can be determined by measuring the resistance between supply pins in this group to determine if the supply pin group qualifies for reduced testing. If measurements are taken, all pin combinations within this supply pin group must be checked to ensure the maximum resistance is verified as less than or equal to 1 ohm.

7.4 CDM Test Recording/Reporting Guidelines

7.4.1 CDM Test Recording

The CDM testing procedure for a particular product shall be recorded and stored per each company's data retention procedure. Information regarding tester waveform parameters should be available upon request; refer to Annex I.3 for more information on waveform parameter recording.

NOTE See the ESDA/JEDEC JTR002-01 User Guide for more info on waveform parameter recording.

7.4.2 CDM Reporting Guidelines

Product CDM test results (including package information) shall be reported and be made available in the product reliability report.

For purposes of ensuring safe handling information for manufacturing control in an ESD protected area, it is highly recommended that publicly available product datasheets report CDM classifications and/or withstand levels. The lowest withstand threshold shall always be reported.

In some cases, it is desirable to report an additional withstand threshold for a subset of pins that is lower or higher than the full set of pins. The procedure for determining and reporting multiple thresholds is described in Annex D.

7.5 Testing of Devices in Small Packages

Integrated circuits and discrete semiconductors (ICDS) in very small packages are very difficult to test for CDM and seldom fail CDM testing due to their small capacitance. It is impossible to specify a package dimension below which CDM testing is not needed as different technologies, design styles, and protection strategies have different susceptibilities to charged device events. In the absence of other information, all ICDS shall be tested. However, Annex C defines an optional procedure for establishing an integrated circuit capacitance C_{Small} for a specific technology and design flow. For devices with capacitance below C_{Small}, CDM testing is no longer required. ICDS with capacitance below C_{Small} and which satisfy the requirements of Annex C shall be considered to have a CDM passing level of TC 750 (Classification Level C2b in Table 3).

8 CDM Classification Criteria

ESD sensitive (ESDS) devices are classified according to the test procedure described in this standard. CDM test results are specific to the particular package type used. The device classification is the highest CDM stress voltage level (both positive and negative polarities) that a sample of at least three devices has passed full static and dynamic testing per data sheet parameters following CDM testing. The CDM ESDS device classification levels are presented in Table 3.

Table 3 — CDM ESDS Device Classification Levels

Classification Level (see Note 1)	**Classification Test Condition (in Volts) (See Note 2)**
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	≥1000 (see Note 3)

NOTE 1 Use the "C" prefix to indicate a CDM classification level.

NOTE 2 The Classification test condition is not equivalent to the actual set voltage of the tester. See Clause 6.5.1 and Annex I for further details.

NOTE 3 For test conditions above 1000 volts, depending on the device package's geometry, corona effects may limit the actual pre-discharge voltage and discharge current.

Annex A (Normative) Verification Module (Metal Disc) Specifications and Cleaning Guidelines for Verification Modules and Testers

A.1 Tester Verification Modules and Field Plate Dielectric

The verification modules (metal discs) shall be made of brass, plated with nickel or gold/nickel, and may optionally have a gold flash coating over the nickel. These shall be manufactured to the dimensions specified in Table 4 and shall be verified by the manufacturer or user before initial use.

One module surface shall always be designated to face the field plate dielectric as described in Annex B. The field plate dielectric is chosen (see Clause 5.1.3) to result in a capacitance measurement in the range specified in Table 4.

Thickness and flatness are illustrated in Figure 3. Thickness is defined as the separation between the two circular faces of the coin. The thickness should be measured near but not at the edge of the coin to avoid false values due to dish or domed surfaces. Surface flatness variation is defined as the distance between two parallel planes containing the entire surface.

NOTE Caution should be exercised during the manufacturing of the modules to avoid "burrs" as these may alter the results.

NOTE Care should be taken to minimize dishing and doming, as illustrated in Figure 3. This is important to ensure compliance with the flatness variation and capacitance specifications in Table 4.

NOTE It is permissible to place an identifying marking on the surface of the module that will always face the pogo pin. This marking may be etched, and the etched region may exceed the surface flatness specification. The marking should be far from the center of the module where the pogo pin makes contact.

Table 4 — Specification for CDM Tester Verification Modules (Metal Discs)

Disk	Small	Large
Diameter mm	8.89 ± 0.127	25.4 ± 0.127
Thickness mm	1.27 ± 0.05	1.27 ± 0.05
Surface flatness variation mm		
Surface contacting the field plate	≤ 0.03	≤ 0.03
Surface contacting the pogo pin	≤ 0.09	≤ 0.09
Capacitance at 1 MHz (pF)	7.2 ± 13%	55 ± 13%

A.1 Tester Verification Modules and Field Plate Dielectric (cont'd)

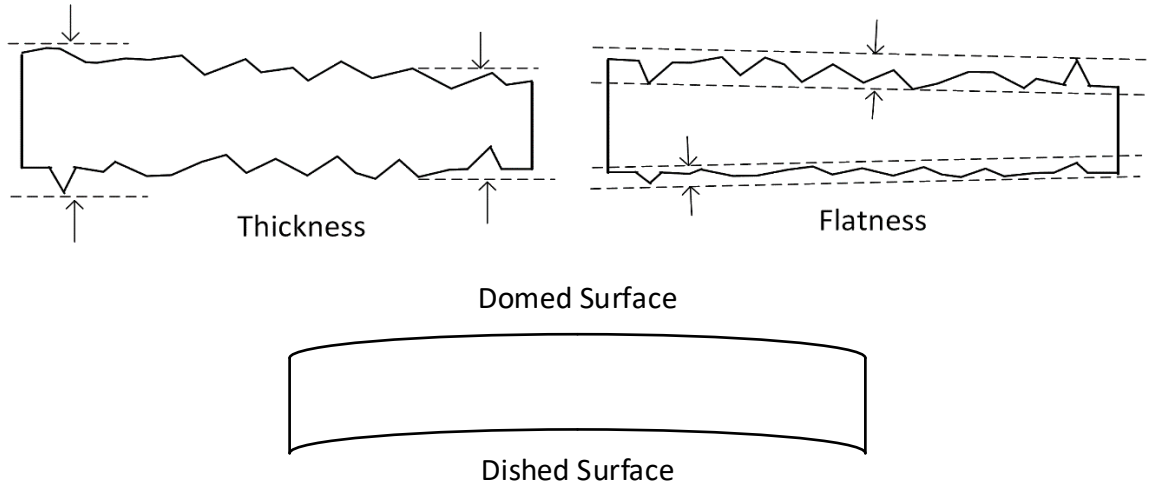


Figure 3 — Verification Module Thickness, Flatness, Dishing, and Doming Illustrations

A.2 Cleaning Requirements

The verification modules should be cleaned (See Clause 7.1.3) using IPA swabs for about 20 seconds as approved by the local safety organization and dried in a moderate air stream. This will prevent charge loss during CDM evaluation. Verification modules should be handled in a way that maintains cleanliness.

The capacitance of the small and large verification modules (metal discs) shall be measured according to the procedure in Annex B and shall conform to the values specified in Table 4.

The tester should be cleaned periodically with IPA to remove any surface contamination resulting in charge loss. Particular attention should be paid to the discharge probe and field plate dielectric on which the device is placed.

NOTE: Cleaning with IPA swabs may leave the surface moist for some time after the cleaning. The moisture may provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning, either by allowing sufficient time for the surfaces to dry or using forced airflow to evaporate the moisture.

Annex B (Normative) Capacitance Measurement of Verification Modules (Metal Discs)

B.1 Capacitance of Verification Module Sitting on Tester Field Plate Dielectric

1) The verification modules' capacitance shall be measured in-situ (inside the CDM tester) but can also be measured outside of the CDM tester as guidance.

2) The small verification module is placed on the dielectric layer, which directly contacts the surface of the grounded metallic field plate. Ensure there is no air space between the module and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate.

NOTE It is recommended that the vacuum be used to ensure the verification module is held firmly against the field plate dielectric.

3) Ensure the capacitance meter is "zeroed out" before measurement. Connect the two leads from the capacitance meter as follows. One metallic lead/cable from the capacitance meter is connected to an exposed point on the field plate. The second metallic lead/cable from the capacitance meter is connected to the verification module's top surface (in the center).

4) Measure the capacitance of the module to the grounded field plate.

5) Flip the module over and repeat step 1) to step 4) with the opposite surface now face down on the field plate. The module orientation that results in the largest measured capacitance shall be identified, and this orientation shall be used for tester verification. The capacitance in this orientation shall be within the value specified in Annex A, Table 4.

NOTE It is permissible to place an identifying marking on the surface of the module that will always face the pogo pin. This marking may be etched, and the etched region may exceed the surface flatness specification. The marking should be far from the center of the module where the pogo pin makes contact.

6) Repeat step 1) to step 5) using the large verification module on the dielectric.

NOTE Parasitic parallel capacitance in the capacitance measurement setup causes an error in the measured capacitance value. A meter with "guarded leads" and a small exposed metal contact is recommended for use.

NOTE The exposed metal contact of the lead touching the verification module may not be small enough to reduce the parasitic parallel capacitance to a negligible level (0.20 pF or less as measured between the lead and the field plate with the lead touching the dielectric). One recommended technique for each verification module is to make a first measurement as in Clause B.1, step 4) and then make a second measurement with the capacitance meter leads hovering approximately 1 mm above the verification module. The second measurement is subtracted from the first to result in a more accurate measured value.

Annex C (Informative) Testing of Small Package Integrated Circuits and Discrete Semiconductors (ICDS)

This annex describes a procedure for setting a capacitance limit C_{small}, below which small package integrated circuits and discrete semiconductors no longer need to be tested for CDM. ICDS in very small packages is very difficult to test due to the challenge of handling small devices. Very small ICDS also have very low capacitance to surroundings, including during CDM testing. With a small capacitance, very little charge is transferred during a CDM event, either in a factory environment or during CDM testing. Small package ICDS therefore, seldom fail during CDM testing. This does not, however, mean that there is no CDM risk for small package ICDS. The charge transferred during a small package CDM event may be small, but the peak currents remain high, usually over an amp since the RLC equivalent circuit of a CDM event results in a very narrow but still high current pulse. It is very difficult to set a minimum package dimension or capacitance for CDM testing because CDM failure levels depend on a wide variety of variables, including those listed here:

- The capacitance between the ICDS and the field plate.
- The technology used to fabricate the device.
  - Advanced low voltage technologies have thin gate oxides with low breakdown voltage and may be more susceptible to CDM damage without a proper protection scheme.
  - High voltage technologies have diffusions which can be subject to CDM damage.
- ESD protection circuits used in the device.
- General ESD protection strategy used.
- Design style used to design the device.
- The thoroughness of ESD design rule checks.
- Package type which can influence inductance in the CDM current path.

NOTE Further information on CDM tester considerations for small packages can be found in the ESDA/JEDEC JTR002-01 User Guide.

C.1 Procedure for Determining C_{Small}

The following procedure may be used to determine a limit, C_{small}, at and below which CDM testing is not required for a particular integrated circuit technology.

- Choose at least 5 ICDS designs from a technology with varying package sizes.
  - The requirements for circuits to be considered from the same technology are given in Clause C.2.
- Measure the capacitance between each ICDS substrate, usually the ground pin, and the CDM tester's field plate when the ICDS is in the position for CDM testing, using the procedure in Annex B for measuring the capacitance of the verification modules.
  - Packages shall be at least four times the size of the vacuum hole in the dielectric layer or the metal field plate, whichever is larger, if it is to be placed over a vacuum hole. If the package is less than four times the vacuum hole's size, a test fixture that holds the package against the dielectric away from the vacuum hole should be used.

C1 Procedure for Determining C_{Small} (cont'd)

NOTE Currently there is no universally recognized method for testing CDM capability on packages that are less than four times the size of the vacuum holes. Techniques such as mechanical fixtures made of FR4 for holding the package (not over vacuum holes) or packaging die in a different package, have been used.

- A separate test fixture may be used for measuring the capacitance if it uses the same thickness and material for the field plate dielectric layer as the CDM tester.

- Perform CDM testing at TC 1000 for three samples as per Clause 7.3.3 for each of the 5 ICDS designs.
- The ICDS capacitance, at which all ICDS with that capacitance and lower all pass CDM TC 1000, is C_{Small}.

NOTE The use of a vacuum is recommended to ensure there is no air space between the integrated circuit and the dielectric layer, and no air space between the dielectric layer and the metallic field plate.

- ICDS with a substrate to CDM tester field plate capacitance equal to or less than C_{Small} do not need to be tested for CDM if the following conditions are met:
  - The ICDS has passed HBM according to the requirements of the technology. This indicates the expected protection circuit is present.
  - The ICDS uses the same technology, as defined in C.2, as used to determine $C_{Small.}$
- ICDS devices not tested because their capacitance is below C_{Small} and satisfy the above requirements shall be considered to have a CDM passing level of TC 750 (Classification Level C2b).

C.2 ICDS Technology Requirements

ICDS is considered to be from the same technology if the following conditions are met:

- The ICDS shall use the same wafer fabrication flow.
- All ICDS shall use the same ESD protection circuits and ESD design rules.
- All ICDS shall have their substrate to CDM tester field plate capacitance measured using the procedures in Annex B.
  - A separate test fixture that simulates the CDM tester field plate and dielectric may be used.
  - The calculated substrate to field plate capacitance may be used if the calculation procedure has been verified with measurements using the procedures in Annex B.

Annex D (Informative) Determination of Withstand Thresholds for Devices to be Reported with Multiple Thresholds

D.1 Introduction

ANSI/ESD SP5.0, "For Electrostatic Discharge Sensitivity Testing: Reporting ESD Withstand Levels on Datasheets", gives recommendations on how to report separate ESD withstand levels for special subsets of pins. This annex provides instructions for performing CDM testing on devices to enable this segmented threshold reporting. This procedure intends to accommodate identification of lower passing levels for pins, which, due to functional requirements, cannot be designed with the same withstand levels as other pins on the device.

This method will likely require prior knowledge of the device's expected pin specific ESD performance levels, such as from design information, from the previous testing using all pins, or testing on other devices or test structures.

In the following procedure and requirement clauses, Levels A, B, C, etc., are either CDM test conditions or classification levels.

NOTE Even when these subsets are determined, the overall device level threshold is still reported based on the lowest threshold pin.

D.2 Testing Procedure

- At Level A, the lowest withstand level to be reported.
  - Stress all pins on three devices as required in Clause 7.0.
  - Verify full functionality, as described in Clause 7.2.2.2. Any pins passing this level may be reported as Level A.
- At Level B, the next higher withstand level to be reported.
  - Stress all pins on three devices as required in Clause 7.0, excluding pins to be reported as Level A.
  - Either new devices or the devices used in Level A testing may be used.
  - Verify full functionality, as described in Clause 7.2.2.2. Any pins passing this level, except those excluded from stressing at Level B, may be listed as Level B.
- At Level C, the next higher withstand level to be reported.
  - Stress all pins on three devices as required in Clause 7.0, excluding pins to be reported as Level A and Level B.
  - Either new devices or the devices used in Level B testing may be used.
  - Verify full functionality, as described in Clause 7.2.2.2. Any pins except those excluded from stressing at Level C may be listed as Level C.
- The procedure may be repeated at additional levels, but it is expected that only two or maybe three levels would be practical for reporting purposes.
- If separate sets of three devices are to be used for the different stress levels, it is permissible to perform the stressing in parallel, followed by complete static and dynamic testing, if the expected withstand levels are known before testing. A part is defined as having a failure according to the criteria listed in Clause 7.2.2.2.

D.3 Restrictions

If all pins pass at level X, but a subset of pins (a, b, c, and d, for example) fail at a higher-level Y with all pins being stressed, it is not permissible to list the failing pins (a, b, c, and d) as level X, with all remaining pins reported as level Y. This is because it is possible that stress to pins other than the failing pin(s) caused the pin failures.

D.4 Example of Using Subset Withstand Threshold Data

This is an example of the use of pin subset threshold data as it appears in ANSI/ESD SP5.0. The example also includes human body model (HBM) pin subset thresholds, which may be reported similarly.

A 20-pin device has been evaluated using ANSI/ESDA/JEDEC JS-002 and ANSI/ESDA/JEDEC JS-001. 18 of the 20 pins pass CDM at 500 volts while two high-speed pins (here designated as pins 3 and 4) only pass 250 volts. Similarly, 18 of the pins pass HBM at 1000 volts while the same high-speed pins (3 and 4) only pass 500 volts. Table 5 describes one way of conveying these results on a datasheet.

Table 5 — Inclusion of Lower ESD Level High-Speed Pin Data

ESD Information for Handling of ESDS in an ESD Protected Area (Required)
CDM (ANSI/ESDA/JEDEC JS-002): CDM Withstand Threshold 250 volts; CDM Class C1 NOTE The CDM withstand threshold is determined by two high-speed pins (3 and 4), which pass 250 volts. All other pins pass 500 volts.
HBM (ANSI/ESDA/JEDEC JS-001): HBM Withstand Threshold 500 volts; HBM Class 1B NOTE The HBM withstand threshold is determined by two high-speed pins (3 and 4), which pass 500 volts. All other pins pass 1000 volts.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex E (Informative) History and Motivation Behind the Creation of a Joint CDM Test Standard

E.1 Background

This joint ESDA/JEDEC CDM standard (ANSI/ESDA/JEDEC JS-002) was first released in 2014. It was developed by a joint working group composed of both ESDA and JEDEC committee members. The joint document was intended to replace the existing charged device model ESD standards that were available from both organizations at the time (JESD22-C101 and ANSI/ESD S5.3.1). It contains the essential elements from both standards. The joint document is intended to reduce duplication of effort and confusion by developing a single joint work in progress. The joint document corrected deficiencies in the CDM standards that existed at the time, and it aimed to maintain similar stress levels as the legacy JEDEC CDM standard since it is the most widely used CDM test method.

E.2 CDM Test Hardware and Metrology Improvements

Merging the two legacy standards required significant hardware and metrology changes to arrive at an improved joint work in progress. This informative annex describes the history and motivations for the changes made to combine the two documents for the first joint release.

The major changes in this test method are listed here.

- Modified details of the required waveforms to better match the high-frequency behavior of CDM events.
- Requires the test head not include ferrites or other circuits to modify the CDM pulse's high-frequency behavior.
- Requires tester qualification and requalification be performed with a 6 GHz or faster oscilloscope and recommends using 6 GHz or faster oscilloscopes for quarterly and regular tester verification if a fast oscilloscope is available.
- The tester qualification and verification procedures have been modified to give more flexibility in the field plate voltage settings to arrive at the required peak currents.
- The specification of test levels by voltage has been replaced by a series of test conditions related to the legacy JEDEC CDM voltage levels.

When the original CDM test method was developed in the late 1980s, single-shot oscilloscopes with 1 GHz and higher bandwidths were expensive, not readily available, and less capable than those available today. The result was that the original waveforms used to develop the JEDEC CDM standard had a wider full width at half height (FWHM) than was characteristic of the actual CDM event. As measurement capability improved and the high-frequency behavior of test heads was improved, tester manufacturers found the peak width at FWHM was narrower than allowed by the JEDEC standard. To meet the peak width at FWHM, ferrite beads were often added to the test head to bring the current waveforms into compliance.

E.2 CDM Test Hardware and Metrology Improvements (cont'd)

When oscilloscopes in the 4 GHz to 8 GHz range became readily available, it was found that the ferrite beads, which broadened the peak width when measured with a 1 GHz oscilloscope, created undesirable high-frequency harmonics with undesirable consequences. A primary goal in developing this standard was to remove the ferrite beads from the CDM test heads and modify the waveform requirements to allow this change.

The 1 GHz oscilloscope specified in the JEDEC standard, and allowed in the ESDA standard, is only marginally fast enough to capture CDM events and significantly reduces the measured peak current of the captured waveforms, especially for the small verification module and small integrated circuits. Accurate peak current measurements require using a measurement chain with 6 GHz or higher bandwidth, and the new Joint Standard reflects this requirement for CDM tester qualification. A 1 GHz oscilloscope was considered adequate for routine waveform verification. That option is still available in the joint standard, although the higher bandwidth oscilloscope is recommended if it is available.

The increased flexibility between the required peak current values and the field plate voltage to produce the peak current has been implemented for two reasons; to better match current practice and achieve similar stress levels as the legacy JEDEC standard.

Both the JEDEC and ESDA standards specified the CDM tester geometry and the required waveforms at specified field plate voltages. CDM tester manufacturers quickly found that it was often impossible to obtain the required peak current values with the required geometry and the specified field plate voltage. The manufacturers introduced adjustments to the field plate voltage so that the required waveforms were obtained when the specified voltage was selected in the CDM tester software. This adjustment was reasonable since it is known that it is peak current, not field plate voltage, which damages integrated circuits. The result was that when an integrated circuit passed 500 volts, the field plate voltage was often considerably different than 500 volts. Still, the intended current pulse was applied to the device under test.

The removal of the ferrite beads and the extra impedance which the beads produced have resulted in higher peak currents than those present in the legacy JEDEC test method for the same field plate voltage and tester geometry. This creates a second reason to give more flexibility in setting the field plate voltage to obtain the required peak currents. Since CDM failure results from the peak current during the CDM event, it is more important that different CDM testers create the same peak current for specified test conditions than that the field plate voltages are the same. For this reason, the test voltages specified in the earlier standard CDM documents have been replaced by a series of test conditions producing peak currents similar to those at the specified voltages in JESD22-C101.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex F (Informative) CDM Tester Electrical Schematic

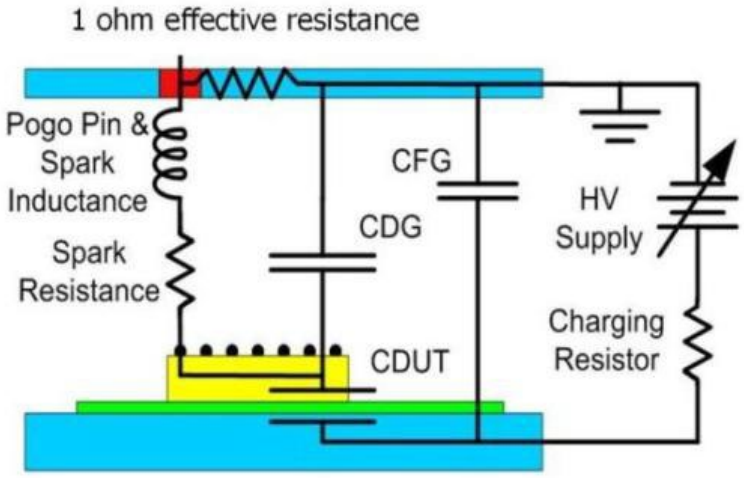


Figure 4 — Simplified CDM Tester Electrical Schematic

Figure 4 represents an electrical model of a CDM tester setup. CDUT is the capacitance between the DUT and the field plate, CDG is the capacitance between the DUT and the ground plane, and CFG is the capacitance between the field plate and the ground plane. When measuring the waveform, the 1 ohm resistance between the pogo pin and the ground plane will be the parallel combination of the resistive probe and the coaxial cable/oscilloscope impedance described above. The spark resistance which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor.

Further information on the CDM tester electrical schematic and package effects can be found in the ESDA/JEDEC JTR002-01 User Guide.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex G (Informative) Sample Oscilloscope Setup and Waveform

The following setup examples are based on a TC 500 waveform measurements using a 1 GHz and 8 GHz oscilloscope. Other oscilloscopes will have different settings, but this annex should provide basic guidelines for most oscilloscopes.

G.1 Settings for the 1 GHz Bandwidth Oscilloscope

Vertical: 200 millivolts/division (small verification module) or 200 millivolts/division (large verification module)

Time base: 400 ps/division

Trigger: 300-millivolt small verification module or 400-millivolt large verification module

Impedance = 50 ohms

NOTE These settings are for an oscilloscope for which the attenuation correction could not be made.

G.2 Settings for the High Bandwidth Oscilloscope

Vertical: 2 volts/division (small verification module) or 2 volts/division (large verification module)

time base: 400 ps/division

Trigger: 3-volt small verification module or 4-volt large verification module

Impedance = 50 ohms

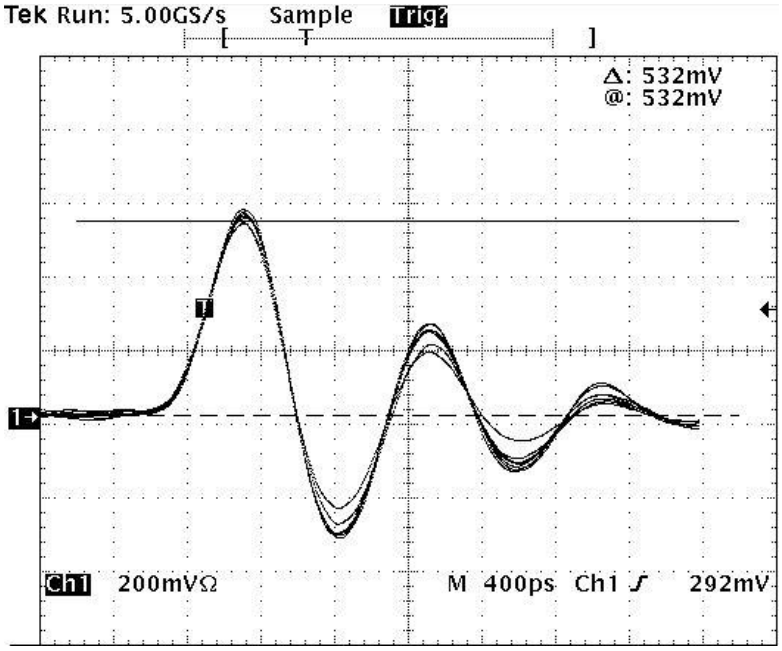
NOTE These settings are for an oscilloscope for which the attenuation correction was made in the oscilloscope software.

G.3 Setup

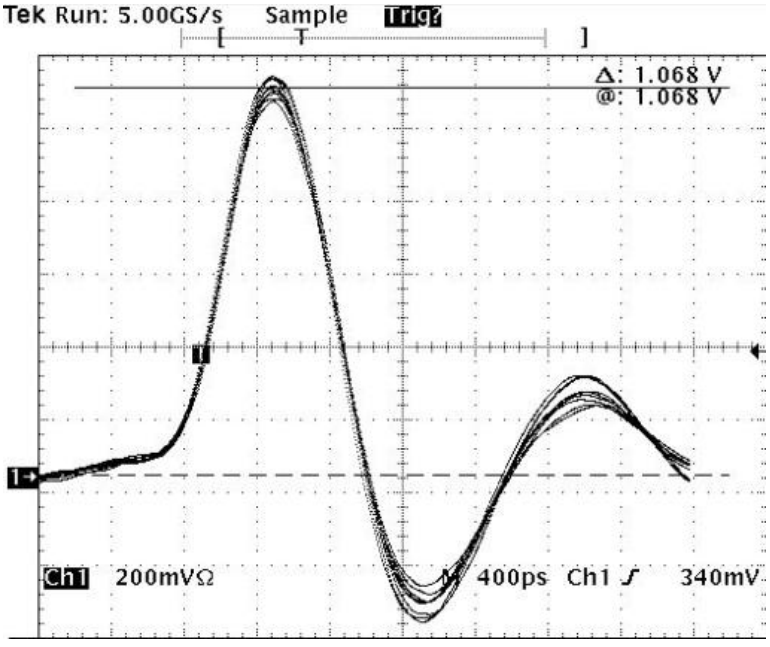
Attach the 20 dB attenuator to the oscilloscope. Attach the cable to the end of the attenuator and the voltage output of the CDM tester.

NOTE The 20 dB attenuator is a 10X attenuator. If the oscilloscope does not automatically compensate for this, the measurements need to be multiplied by 10 to get the correct reading. For example, from a small coin below 532 millivolts translates to 5.32 volts when accounting for the attenuator. This voltage is then divided by the effective resistance of the disk resistor in parallel with the 50 ohm cable and termination to translate to current. Hence, if the effective resistance of the disk resistor and parallel 50 ohm cable were 1.03 ohms, 5.32 volts / 1.03 ohms = 5.17 amperes.

G.4 Sample Waveforms from a 1 GHz Oscilloscope



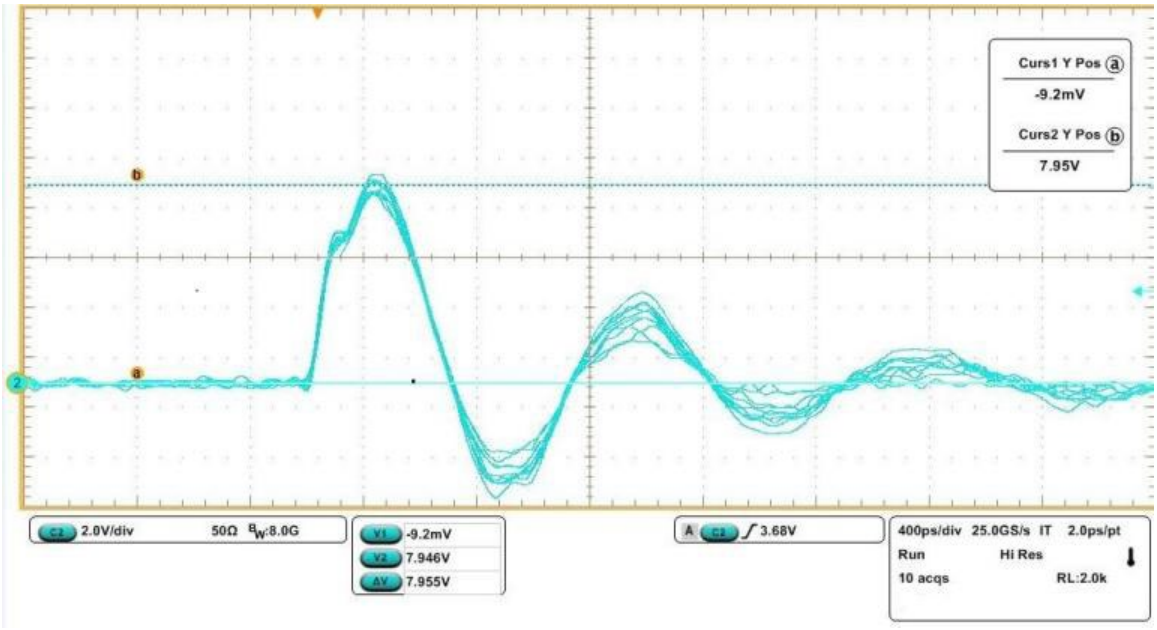
1 GHz TC 500, Small Verification Module



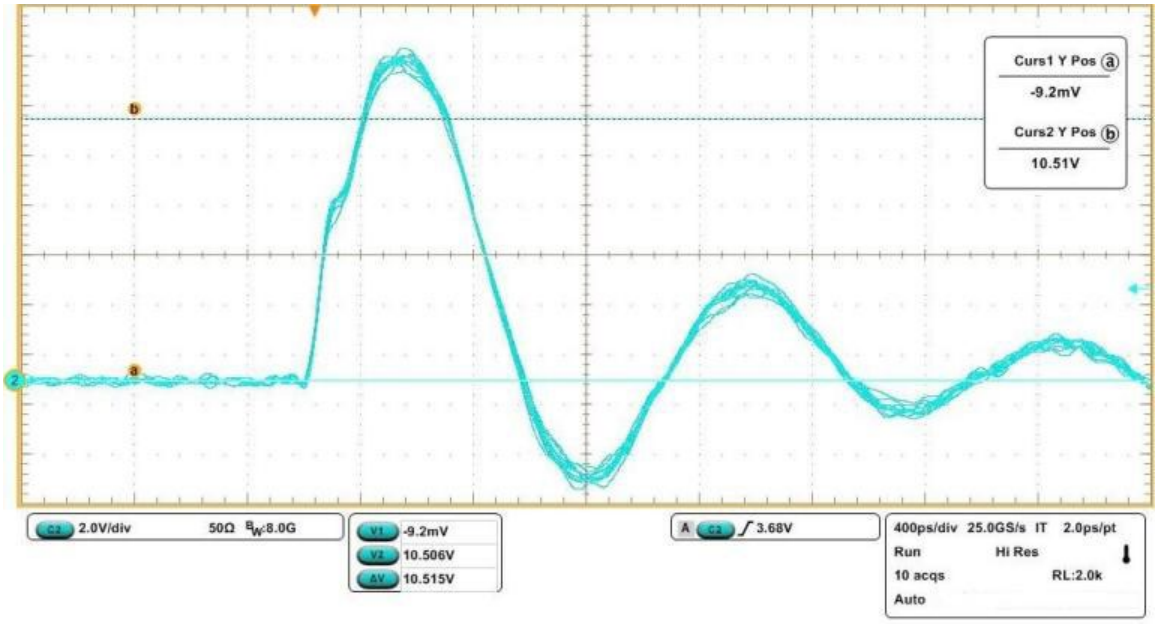
1 GHz TC 500, Large Verification Module

Figure 5 — Sample Waveforms from a 1 GHz Oscilloscope

G.5 Sample Waveforms from an 8 GHz Oscilloscope



8 GHz TC 500, Small Verification Module (Oscilloscope Adjusts for Attenuation)



7 GHz TC 500, Large Verification Module (Oscilloscope Adjusts for Attenuation)

Figure 6 — Sample Waveforms from an 8 GHz Oscilloscope

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

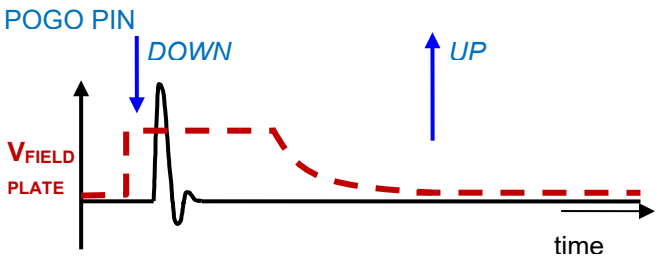
Annex H (Informative) Field-Induced CDM Tester Discharge Procedures

This annex describes the two types of discharge procedures used in field-induced CDM test equipment. Further information regarding the application to no-connect pins can be found in the ESDA/JEDEC JTR002-01 User Guide.

H.1 Single Discharge Procedure

The single positive and single negative discharges can be applied with two individual discharges using this sequence of steps producing the sequence of charging/discharging events, as illustrated in Figure 5.

a. Place the uncharged DUT on the field plate and align it.
b. The field voltage is established by raising the field plate's voltage to the specified stress level.
c. The first discharge is made by lowering the pogo pin to the DUT (see Figure 5).
d. The pogo pin continues to descend until it makes physical contact with the device pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.
e. Then, the voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.
f. The pogo pin is returned to its starting (separated) position (see Figure 5) before the voltage of the same or opposite polarity is applied to the field plate for subsequent discharges.
g. Repeat for each pin to be tested.



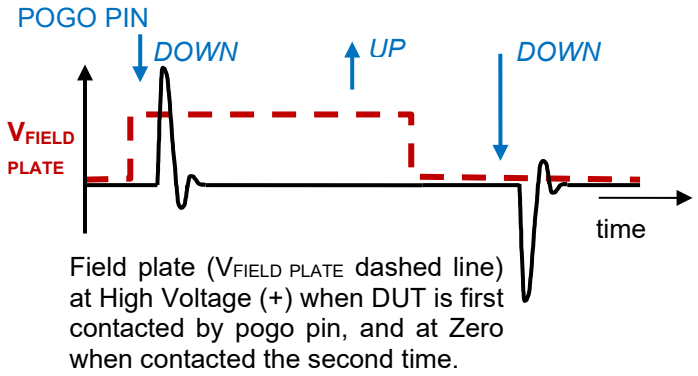
Field plate ($V_{FIELD\ PLATE}$ dashed line) at High Voltage (+) before DUT is contacted by pogo pin, and at Zero before raising the pogo pin

Figure 7 — Single Discharge Procedure (Field Charging, I_{CDM} Pulse, and Slow Discharge)

H.2 Dual Discharge Procedure

Both single positive and single negative discharges can be applied for connected pins, with one pair of alternating polarity discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure 6. For no-connect pins, each dual discharge procedure will result in a single polarity stress only.

a. Place the uncharged DUT on the field plate and align it.
b. The field voltage for the positive stress is established by raising the field plate's voltage to the specified stress level.
c. The first discharge is made by lowering the pogo pin to the DUT (see Figure 6).
d. The pogo pin continues to descend until it makes physical contact with the PUT. This is to ensure full charge transfer and to provide a conduction path to ground.
e. The pogo pin is returned to its starting separated position (see Figure 6), leaving the device with a net charge.
f. The voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.
g. The pogo pin is lowered (the second down arrow to the right in Figure 6) a second time for the second discharge, which will be of opposite polarity and the same magnitude.
h. Repeat for each pin to be tested.



NOTE Field charging 1st I_{CDM} Pulse, No Field, 2nd I_{CDM} Pulse.

Figure 8 — Dual Discharge Procedure

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex I (Informative) Waveform Verification Procedures Using Factor/Offset and Software Voltage Adjustment Methods

NOTE Additional information regarding waveform verification procedures can be found in ESDA/JEDEC JTR002-01 User Guide.

I.1 Factor/Offset Adjustment Method

This procedure aligns the tester for direct software voltage input of the test condition for the full alignment range. This method may not allow for alignment of each test condition with the target mid-range of Ip, as shown in Table 1 or Table 2. Still, it is the easiest to use in a lab environment with multiple testers because the software voltage entered matches the test condition target level and does not require linear interpolation/extrapolation for test conditions other than the five levels listed in Table 1 or Table 2.

The requirements/details of this method are as follows:

- A single factor/offset is used across the entire test condition range.
- A different factor/offset can be used for each polarity.
- The same factor/offset must be used for both large and small verification modules.

Figure 7 depicts the waveform verification flow for qualification/requalification and quarterly checks, while Figure 8 shows the flow for routine verifications. Annex I.3, Table 6, shows an example of the data which should be recorded.

I.1 Factor/Offset Adjustment Method (cont'd)

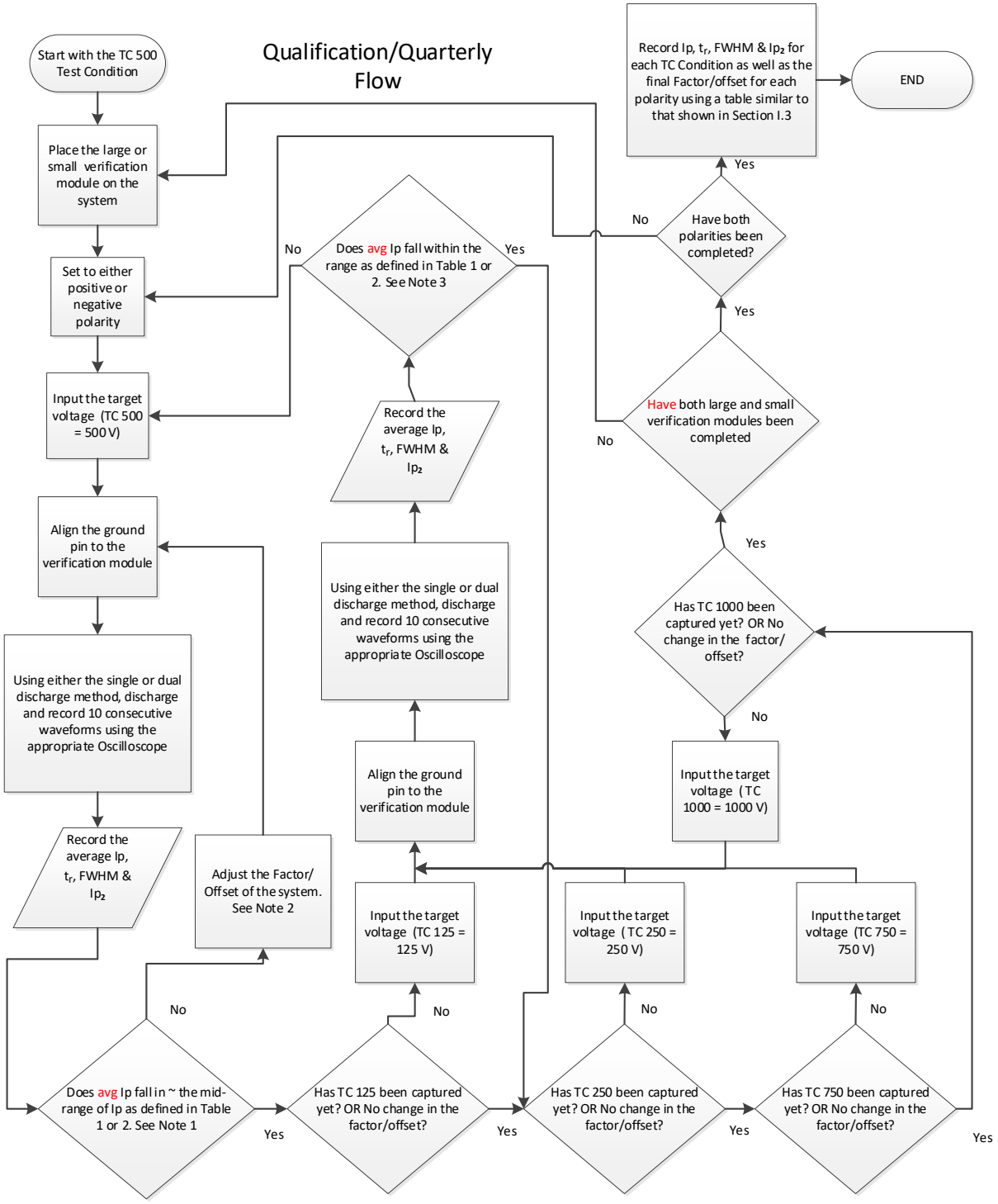


Figure 9 — Example of a Waveform Verification Flow for Qualification and Quarterly Checks Using the Factor/Offset Adjustment Method

I.1 Factor/Offset Adjustment Method (cont'd)

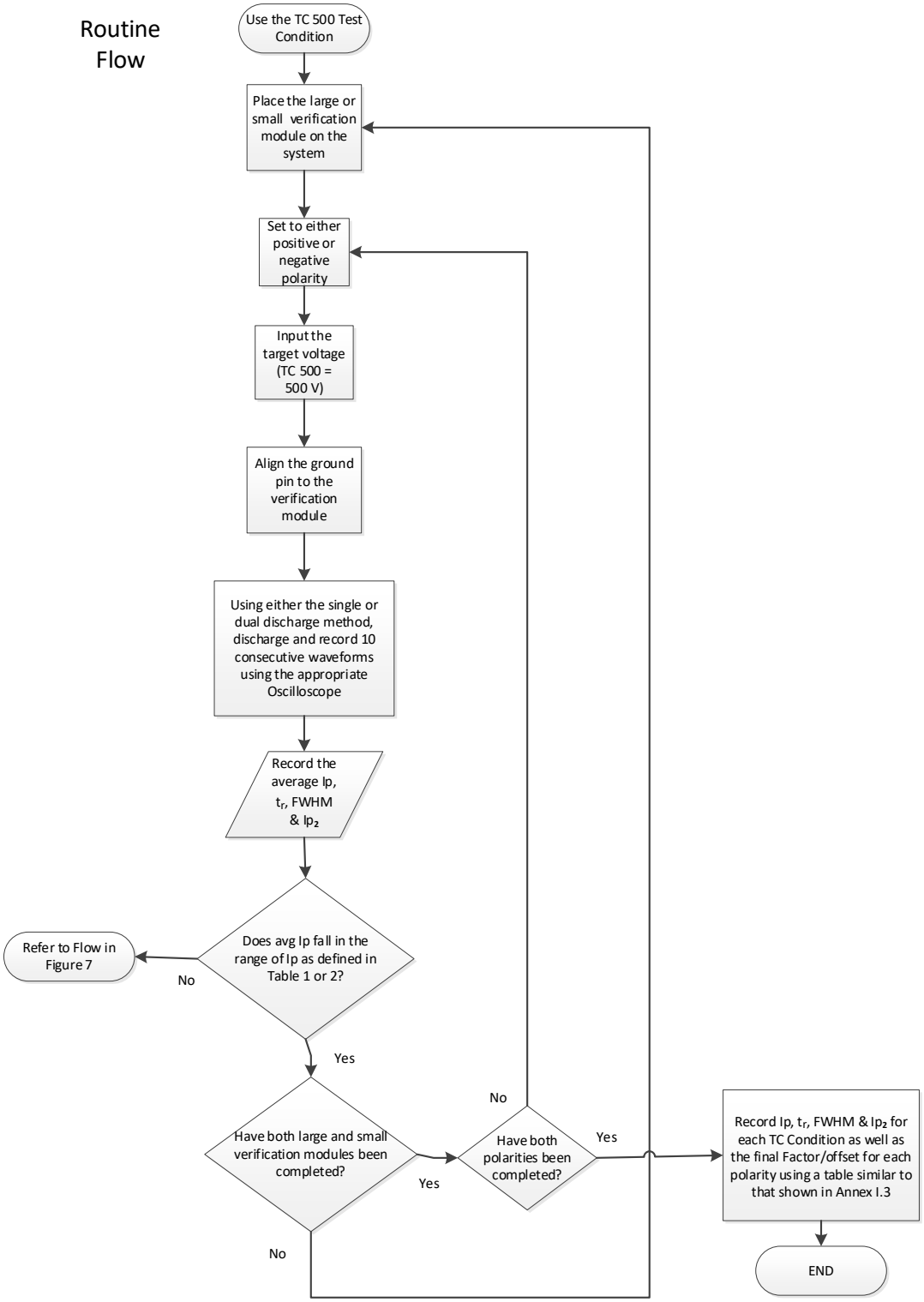


Figure 10 — Example of a Waveform Verification Flow for the Routine Checks
Using the Factor/Offset Adjustment Method

I.1 Factor/Offset Adjustment Method (cont'd)

NOTE Targeting to the mid-range of TC 500 is a starting point for adjusting the field plate voltage. Based on the results of the other test conditions (TC 125/250/750/1000), the Ipeak may end up higher or lower than the mid-range value on TC 500. As shown in Figure 9, adjustments in the factor/offset may shift the Ipeak higher or lower.

NOTE To properly calibrate systems, tester manufacturers have implemented a secondary "adjustment" parameter as an offset from the software voltage setting, either represented as a voltage "multiplier" value or a percentage "offset" value, which modifies the field plate voltage. Consult the tester manufacturer for more detail.

NOTE After several iterations through this loop, if the user finds they cannot meet the Ipeak range as defined in Table 1 or Table 2 or the factor/offset is outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or replace the ground pin. Consult the tester manufacturer for more information.

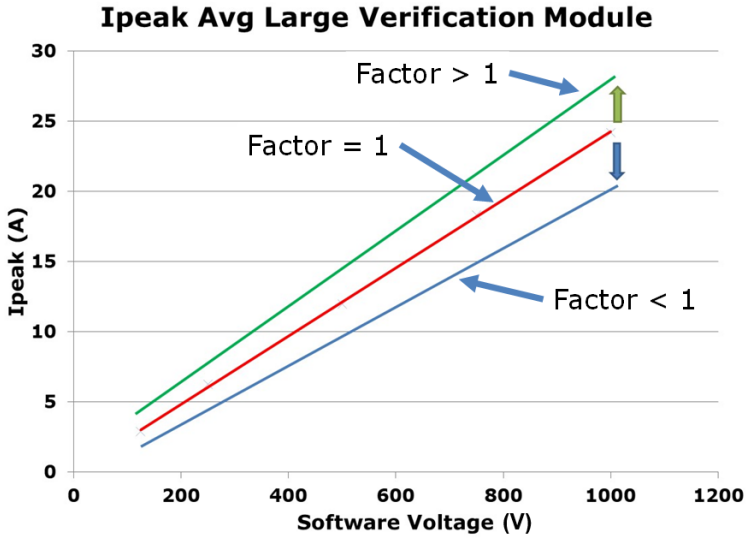


Figure 11 — Example of the Impact of Factor Adjustment on the Average Ip for the Large Verification Module High Bandwidth Oscilloscope

I.2 Software Voltage Adjustment Method

This procedure does not adjust the factor/offset but leaves the factor/offset with a value that will not impact the field plate voltage and uses the software voltage entry as the primary adjustment of the field plate voltage. This method will allow for much more accurate targeting of the Ip range's midpoint as defined in Table 1 or Table 2 but creates complexity in determining the correct software voltage entry between the five test conditions. Determining software voltage entries other than the five test condition levels (which will be determined in this procedure) will require linear interpolation/extrapolation.

I.2 Software Voltage Adjustment Method (cont'd)

The requirements/details of this method are as follows:

- A unique software voltage setting is determined for each test condition.
- Unique voltage settings may be used for each polarity (at each test condition).
- The same software voltage setting must be used for both large and small verification modules at each test condition.
- Testing at levels other than the five test conditions will require a linear interpolation/extrapolation to determine the correct software voltage entry.

Figure 10 depicts the waveform verification flow for qualification/requalification and quarterly checks, while Figure 11 shows the flow for routine verifications. Annex I.3, Table 7, shows an example of the data which should be recorded.

I.2 Software Voltage Adjustment Method (cont'd)

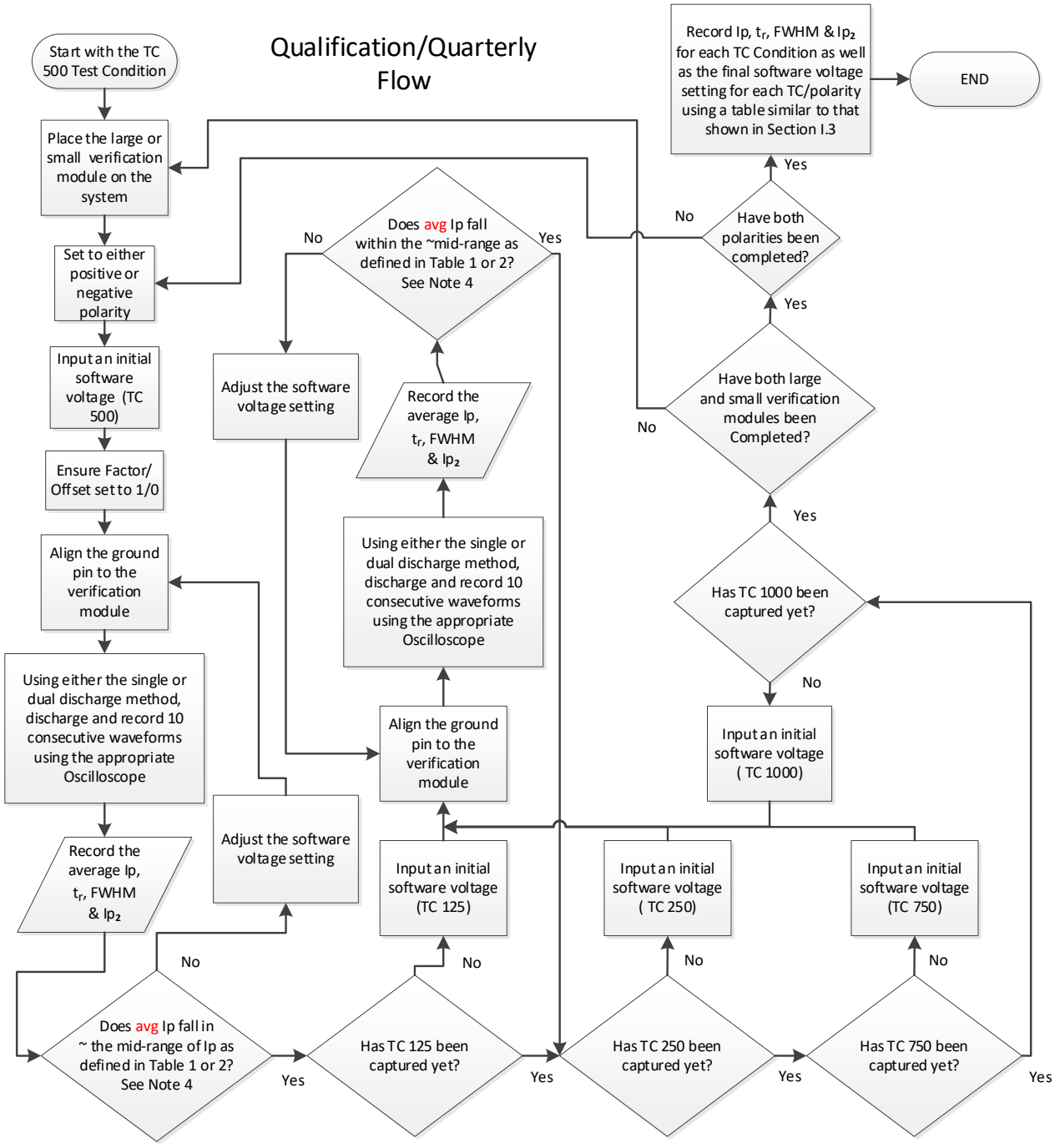


Figure 12 — Example of a Waveform Verification Flow for Qualification and Quarterly Checks Using the Software Voltage Adjustment Method

I.2 Software Voltage Adjustment Method (cont'd)

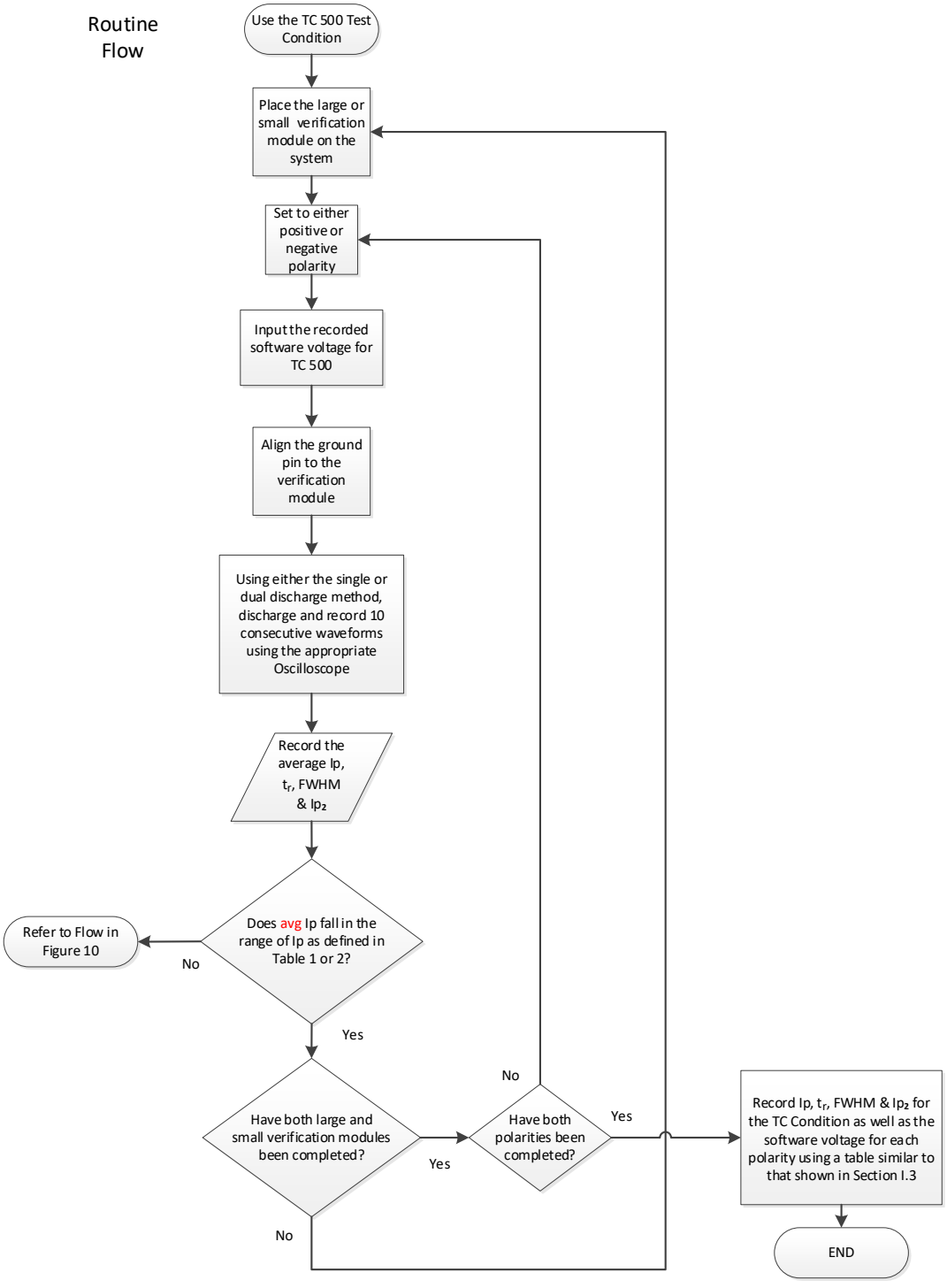


Figure 13 — Example of a Waveform Verification Flow for the Routine Checks Using the Software Voltage Adjustment Method

I.2 Software Voltage Adjustment Method (cont'd)

NOTE After several iterations through this loop, if the user finds they cannot meet the Ipeak range as defined in Table 1 or Table 2, or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or replace the ground pin. Consult the tester manufacturer for more information.

I.3 Example Parameter Recording Tables

Table 6 is an example table of CDM qualification/quarterly verification waveform parameters to be recorded for the factor/offset adjustment method.

Table 6 — Example Waveform Parameter Recording Table for the Factor/Offset Adjustment Method

Tester - System #1									
Polarity = Positive		Scope Bandwidth = 8 GHz				Factor/Offset Final Setting = 0.82			
MODULE SIZE	DATE	%RH	Test Condition	Software voltage (V)	Ip AVG (A)	t_r (ps)	FWHM (ps)	Ip_2 AVG (A)	Ip_2 (% Ip)
Large	dd/m/yy	X%	TC 500	500	12.1	275	610	4.3	36%
Small	dd/m/yy	X%	TC 500	500	7.30	185	400	3.7	51%
Large	dd/m/yy	X%	TC 125	125	2.90	283	611	1.1	38%
Small	dd/m/yy	X%	TC 125	125	1.90	201	395	1.1	58%
Large	dd/m/yy	X%	TC 250	250	6.00	276	609	2.2	37%
Small	dd/m/yy	X%	TC 250	250	3.70	186	397	2.1	57%
Large	dd/m/yy	X%	TC 750	750	18.30	274	611	7.2	39%
Small	dd/m/yy	X%	TC 750	750	11.00	190	398	6.1	55%
Large	dd/m/yy	X%	TC 1000	1000	24.40	276	612	9.2	38%
Small	dd/m/yy	X%	TC 1000	1000	14.60	187	399	7.4	51%

Table 7 is an example table of CDM qualification/quarterly verification waveform parameters recorded for the software voltage adjustment method.

Table 7 — Example Waveform Parameter Recording Table for the Software Voltage Adjustment Method

Tester - System #2									
Polarity = positive		Scope Bandwidth = 8 GHz				Factor/Offset Final Setting = 0.82			
MODULE SIZE	DATE	%RH	Test Condition	Software voltage (V)	Ip AVG (A)	t_r (ps)	FWHM (ps)	Ip_2 AVG (A)	Ip_2 (% Ip)
Large	dd/m/yy	X%	TC 500	410	12.1	275	610	4.3	36%
Small	dd/m/yy	X%	TC 500	410	7.30	185	400	3.7	51%
Large	dd/m/yy	X%	TC 125	105	2.90	283	611	1.1	38%
Small	dd/m/yy	X%	TC 125	105	1.90	201	395	1.1	58%
Large	dd/m/yy	X%	TC 250	205	6.00	276	609	2.2	37%
Small	dd/m/yy	X%	TC 250	205	3.70	186	397	2.1	57%
Large	dd/m/yy	X%	TC 750	620	18.30	274	611	7.2	39%
Small	dd/m/yy	X%	TC 750	620	11.00	190	398	6.1	55%
Large	dd/m/yy	X%	TC 1000	840	24.40	276	612	9.2	38%
Small	dd/m/yy	X%	TC 1000	840	14.60	187	399	7.4	51%

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex J (Informative) Determining the Appropriate Charge Time (Delay) for Full Charging of a Large Module or Device

This annex describes the procedure for characterizing the charge time on the CDM tester and determining the appropriate charge time (for full charging) as either the default charge time for the system (if the initial large verification module checkout fails as described in Clause 6.9) or the charge time required for a very large package device.

J.1 Procedure for Charge Time (Delay) Determination

Follow this procedure to determine an appropriate charge delay.

Using the large verification module or the ground pin of a very large package device:

1. Set the field plate voltage at + 250 volts (any voltage can be used as the objective is to monitor Ip).
2. With the charge time set to 0 ms, collect ten waveforms, and record the Ip from each. Calculate the average Ip of the waveforms.
3. Increase the charge time by 50 ms, collect ten waveforms, record the Ip from each, and calculate their average Ip.
4. Continue incrementing the charge time by 50 ms (a larger or smaller step can be chosen) and record the average Ip until a minimum of 500 ms charge time.
5. Plot the results, as shown in Figure 12.
6. The appropriate charge time results in a "saturation point" for the Ip. As shown in Figure 12, the Ip for this example saturates at ~300 ms. Adding some guard band to this example would ensure a charge time (delay) of 400 ms would be sufficient as either the default charge time on the system (if the large verification module had been used) or as the required charge time on a specific large package device if a large device had been used as the vehicle for the data collection.
7. It is expected that 500 ms will be sufficient for most large devices to reach a saturation point. However, if after 500 ms, a saturation point has not been reached, repeat step 4 and step 5 until this occurs.
8. It is important to note that longer charge times do not "overcharge" the device but would only increase test time.

J.1 Procedure for Charge Time (Delay) Determination (cont'd)

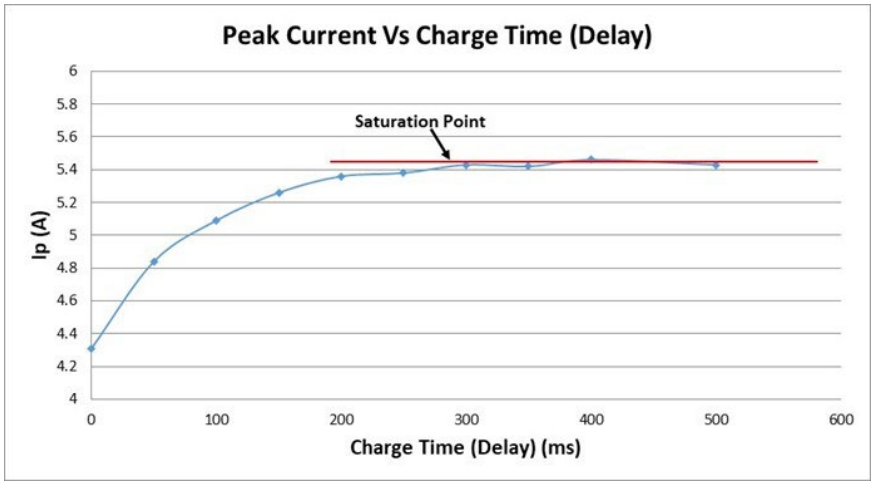


Figure 14 — Example Characterization of Charge Time (Delay) Versus Ip

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex K (Informative) Bibliography

ESDA/JEDEC JTR002-01-21, “User Guide of ANSI/ESDA/JEDEC JS-002”.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-002-2022)

Annex L (Informative) Revision History for ANSI/ESDA/JEDEC JS-002

L.1 Joint Document Summary

The initial version of this standard was a harmonized combination of ANSI/ESD S5.3.1-2009 and JEDEC JESD22-C101F documents. It was intended to replace these and all previous versions. The merged document contains many essential elements of both documents and hardware/measurement modifications, as outlined in this clause.

L.2 ANSI/ESDA/JEDEC JS-002-2014: Summary by Clause

1 **Scope and Purpose –** The scope and purpose of the two documents were merged.

2 **Referenced Documents –** The previous ESDA and JEDEC methods were referenced. The ESDA and JEDEC Glossaries were referenced.

3 **Definitions –** Definitions from ESDA and JEDEC Glossary of Terms were used as appropriate.

4 **Personnel Safety –** this was made a main clause to follow the Definitions clause.

5 **Apparatus and Required Equipment –** This clause was rewritten. Descriptions of the oscilloscope and current transducers were refined. The CDM tester hardware and circuit schematic descriptions were rewritten and improved.

6 **Stress Test Equipment Qualification and Routine Verification –** This clause was completely rewritten. The waveform parameters Clause 6.7 now contains 1 GHz and high bandwidth (≥ 6 GHz) oscilloscope waveform parameters. A procedure for determining if a module or device needed a pre-charge delay setting for the full module/device charging was written and references Informative Annex H.

7 **Classification Procedure –** The basic procedure for sampling, pin combinations, and stressing were similar in both documents. Conditions for humidity were refined. The failure criterion previously in a separate clause in both documents was moved into this clause. A reporting clause was also added.

8 **Classification Criteria –** This clause was rewritten to restate classification levels in terms of test conditions. A 750-volt level was added.

Annex A – This Normative Annex contains verification module specifications from the JESD22- C101F document.

Annex B – This Normative Annex describes capacitance measurement for the small and large JEDEC style verification modules (metal discs) measurement.

Annex C – A new Informative Annex describing the major document changes and reasoning for them was written.

Annex D – A new Informative Annex describing the major elements of the CDM tester electrical schematic was created.

Annex E – This is a new Informative Annex regarding the oscilloscope setup for CDM measurement.

L.2 ANSI/ESDA/JEDEC JS-002-2014 (cont'd)

Annex F – This new Informative Annex describes the single and dual discharge procedures. This information was moved from the CDM Test Procedure clauses of ESDA and JEDEC standards**.**

Annex G – A new Informative Annex was added, describing waveform verification procedures based on test condition voltage settings.

Annex H – A new Informative Annex was added describing the procedure for determining any added pre-charge delay needed to charge a device fully.

Annex I – A revision history Informative Annex was created.

L.3 ANSI/ESDA/JEDEC JS-002-2018: Summary by Clause

3 Definitions – Definition for $\mathbf{C_{Small}}$ was added.

5.2.1 Cable Assemblies – The frequency value was changed to 5 GHz.

6.5.1 CDM Test Qualification/Requalification Procedure – Clarified to only use Table 2.

7.1 Tester and Device Preparations – Clause title changed, sub-clause 7.1.3 and sub-clause 7.1.4 were added to the document to clarify the cleaning of devices and testers.

7.4 CDM Test Recording/Reporting Guidelines – This clause was divided into two sub-clauses - 7.4.1 CDM Test Recording and 7.4.2 CDM Reporting Guidelines.

7.5 Testing of Devices in Small Packages – This clause was added to the document.

Annex A – "shall" changed to "should" in a note.

Annex C – A new Normative Annex was created.

Subsequent annexes were renumbered accordingly.

L.4 ESDA/JEDEC JWIP-002-2022: Summary by Clause

All length/width/height measurements – changed to metric only.

ESDA/JEDEC JTR002-01 – the term "see the ESDA/JEDEC JTR002-01 User Guide" was added as informational text in clauses where more detail on a condition is provided in the new User Guide.

FOREWORD – Foreword was updated to include the following:

New information includes a procedure to determine multiple level CDM withstand thresholds for subsets of device pins and a more accurate definition of verification module physical characteristics and capacitance measurement/use of modules. A companion technical report document, ESDA/JEDEC JTR002-01, has also been released to act as a "user guide" for this CDM test standard.

3 Definitions – Definitions for APL, supply pin, and no-connect pin were added.

5.1.3 Field Plate Dielectric – changed units to metric only; tolerance ± symbol removed from units.

6.9 Procedure for Evaluating Full CDM Tester Charging of a Device – Notes for charge time (delay) were added to this clause, and the charge time terms were used in place of delay in this clause.

7.1.3 Added header **Tester Cleaning**, and a new sub-clause.

7.1.4 Device Cleaning was added.

L.4 ESDA/JEDEC JWIP-002-2021 (cont'd)

7.3.4 Field-Induced Charging Method – Clarified dual discharge procedure (with reference to informative Annex H) that stressing no-connect pins with this procedure will not charge them to the opposite polarity by the first discharge.

7.3.5 Allowance for Reduced Testing on Large Supply Pin Groups – New sub-clause describing allowance (and conditions for allowance) for stressing as few as ten pins of a supply pin group having greater than ten pins.

7.4.2 CDM Reporting Guidelines – Added reference to new Annex D for reporting multiple level thresholds.

Annex A – Changes were made to the physical dimensions/tolerances of the small and large verification modules and the capacitance values/tolerances. Added Figure 3, which shows the verification module flatness. All subsequent figures in the document were renumbered sequentially upward.

Annex B – Changes were made to the capacitance measurement procedure of the verification modules, including a requirement that the side with the highest capacitance is used as the measurement side.

Annex D – A new Normative Annex was created to report withstand thresholds for multiple withstand thresholds of devices.

Subsequent annexes were renumbered accordingly.

Annex E – Updated Annex E to reduce historical content.

Annex G – Corrected NOTE at end of Clause G.3 to account for measurement value of 1 ohm discharge resistor to calculate actual Ip.

Annex I – Updated existing flowcharts correcting waveform parameter symbols. Corrected Table 6 and Table 7 reference to Ip1 changing to Ip.

Annex K – New annex added as a bibliography. Annex K becomes Annex L (revision history).

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Standard Improvement Form JEDEC JS-002-2022

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

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